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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/674,444	10/31/2000	Symon Reuben Brewer	78501 (32-126 USPCT)	9030
27975	7590	08/09/2006		EXAMINER FILE, ERIN M
ALLEN, DYER, DOPPELT, MILBRATH & GILCHRIST P.A. 1401 CITRUS CENTER 255 SOUTH ORANGE AVENUE P.O. BOX 3791 ORLANDO, FL 32802-3791			ART UNIT 2611	PAPER NUMBER

DATE MAILED: 08/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/674,444	BREWER, SYMON REUBEN
	Examiner	Art Unit
	Erin M. File	2611

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 31 July 2006.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-3,5-12 and 15-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-3,5-12 and 15-23 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 31 October 2000 is/are: a) accepted or b) objected to by the Examiner. Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: _____

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-3, 5-12, and 15-23 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1, 2, 5-11, 15-17, 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamre (U.S. Patent No. 5,481,563) in view of Kanack et al. (U.S. Patent No. 6,263,034).

Claims 1, 10, 15, Hamre discloses received digital data (abstract, line 3) which has an offset reference clock offset offset by predetermined frequency amount (abstract lines 3-6 refers to a programmable delay element, fig. 3, 36, although Hamre discloses a time offset and not a frequency offset, the frequency offset if the change in time divided by the period, which can be derived from the time delay), the offset reference clock moves relative to transition point for bits of the digital signal (the recovered clock signal is

generated from the data signal, which is equivalent to the offset reference clock moving relative to transition point for bits in the digital signal, col. 2, lines 51-54). Further Hamre meets the limitation of sampling the signal at sampling times determined by an integer multiple of the frequency of offset reference clock signal, as the recovered clock signal is used to establish a first sampling time for sampling the self-clocking data signal, the sampling interval times are a function of the delay value of the clock offset (col. 2, lines 54-60). Hamre discloses where absent jitter and offset detecting and counting the number of times in any bit different from a predetermined number and counting occasions over predetermined time and using this number to derive a measure of jitter through a circuit means arranged to produce an error ratio signal indicative of the number or count of induced error signals within a defined interval, where the error ratio signal is then compared with a predetermined error ratio value with the results of the comparison being used to control the delay value of the programmable delay means whereby the error ratio signal made to substantially correspond to the adjustable reference signal (col. 2 line 61 – col. 3, line 5).

Hamre fails to disclose a jitter free offset reference clock formed from an offset digital signal, however, Kanack discloses an offset clock which is formed in response to a digital signal to create a reference clock in which the phases of the clock signal are spaced at known intervals in order to reduce jitter (col. 4, lines 25-26, 33-42, this teaches towards the elimination of jitter, hence, a jitter free clock). Kanack further discloses the reference clock of the voltage controlled oscillator (col. 4, lines 21-22) is input into sampling latch 50 to sample the digital signal (col. 4, line 50, fig. 2, 50, 48).

The reduction of jitter in a clock has the advantage of creating a more stable and reliable data output and would therefore be obvious to one skilled in the art at the time of invention to incorporate the digital jitter free clock as disclosed by Kanack into the invention of Hamre.

Claims 2, 17, Hamre further discloses offset reference clock signal is formed by extracting a clock signal from said digital signal and offsetting said clock signal by said predetermined frequency (col. 2 lines 51-60).

Claim 5, 16, 20, Hamre discloses sampling the times are at clock bit intervals being plus and minus one of said integer multiple (col. 2, 56-60).

Claims 6, 15, 19, although Hamre fails to disclose the method of determining a sampling period, using the inverse proportion of the bit rate and higher frequency offset is a design choice and simply represents using the original clock frequency (bit rate) and some offset.

Claims 7, 21, Hamre discloses wherein one of said at least one measure of jitter is obtained by counting up one value for each of said occasions representing sampling times greater than the predetermined number within a bit, counting down one value for each of said occasions representing sampling times less than the predetermined number within a bit and determining the difference between the maximum count value and the minimum count value (col. 2, lines 64-67).

Claims 8, 22, Hamre discloses wherein one of at least one measure of jitter is obtained by counting up one value for each of said occasions representing sampling times greater than the predetermined number within a bit, counting down one value for each

of said occasions representing sampling times less than the predetermined number within a bit and determining the time difference between the first occasion of the maximum count value and the last occasion of the minimum count value (col. 2, lines 64-67).

Claims 9, 23, the further limitation of dividing the time difference by said integer multiple and said predetermined time meets the definition of the frequency offset determination as met in claim 1 above.

Claim 11, Hamre further discloses means for forming the offset reference clock comprises extracting the clock from the digital signal and offsetting the clock signal (col. 2, lines 51-60).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 3, 12, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamre (U.S. Patent No. 5,481,563) and Kanack et al. (U.S. Patent No. 6,263,034) as applied to claims 1, 11, and 17 above, and further in view of Yoshimura (U.S. Patent No. 6,100,724).

Claims 3, 12, 18, inherit the limitations of Claims 1, 11, and 17 respectively. Neither Hamre nor Kanack disclose smoothing the reference clock. However, Yoshimura discloses a phase comparator (fig. 2, 5) for calculating a phase difference by using sampled values before and after an edge portion of the signals outputted from the A/D converter (fig. 2, 4), a filter (6) for smoothing the phase difference outputted from the phase comparator (fig. 2, 5) so as to output a signal converted into a direct current, a variable frequency oscillator (fig. 2, 7) for reproducing a synchronous clock on the basis of the signal-outputted from the filter (fig. 2, 6), a jitter measuring section (fig. 2, 9) for detecting a jitter detection signal on the basis of unevenness of the phase difference obtained by the phase comparator (fig. 2, 5, col. 3, lines 12-24). Because smoothing the reference clock can result in more accurate phase measurements, resulting in improved jitter measurement, it would be obvious to one skilled in the art at the time of invention to incorporate the clock smoothing of Toshimura into the invention of Hamre.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erin M. File whose telephone number is (571)272-6040. The examiner can normally be reached on M-F 10:00-6:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Erin M. File



5/1/2006



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SUPERVISORY PATENT EXAMINER